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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yasuhiko INAGAKI, et al.

Serial No.: 10/615,232

Group No.: 2838

Filed: July 8, 2003

Examiner: B. Vu

For: POWER SUPPLY CIRCUIT CAPABLE OF EFFICIENTLY SUPPLYING A
SUPPLY VOLTAGE

Attorney Docket No.: U 014709-8

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR NEW ACTION

A new Action is requested to consider the Information Disclosure Statement and
Amendment of December 5, 2006.

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8a)

I hereby certify that this correspondence is, on the date shown below, being:

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Date: December 20, 2006


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William R. Evans
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REMARKS

The Action of December 7, 2006, fails to consider claim 5 as a whole.

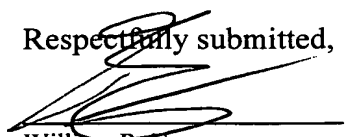
**THE CLAIMED INVENTION AS A WHOLE
MUST BE CONSIDERED *MPEP* 2141.02 I**
(emphasis original)

The whole of claim 5 has a bootstrap circuit that heightens an input impedance "of" the output circuit, and not -- to -- the output circuit as in the Berringer, et al. patent. The whole claimed invention includes even its shortest words.

The Action still slights this distinction by using reference characters for the delay circuit (21, 22) and bootstrap circuit (15), but not for the output circuit.

The applicant traverses this slight by pointing out again that the output circuit must be on the right of Fig. 1 of the Berringer, et al. patent in order to generate, as claimed, the supply voltage delayed by the delay circuit (21, 22) that is in the middle in the patent. In the patent, the bootstrap circuit (15) may heighten an impedance, e.g., from input 38 -- to -- the output circuit, but is in the wrong place to heighten an input impedance "of" the output circuit, as claimed. To be "of" the output circuit, the bootstrap heightener must be with the output circuit on the right, and it's not; it's on the left.

Respectfully submitted,



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